

A cross-sectional view of a semiconductor device. A substrate 20 is shown with a gate stack 24 on top. The gate stack 24 includes a gate dielectric layer 22 and a gate conductive layer 23. A conductive layer 26 is formed on the gate stack 24, with a central portion 27. The conductive layer 26 has a top surface 28A and a bottom surface 28B. The width of the central portion 27 is indicated by L1, and the width of the conductive layer 26 is indicated by L2. A contact pad 21 is formed on the substrate 20, and a contact pad 25 is formed on the conductive layer 26.

FIG. 3

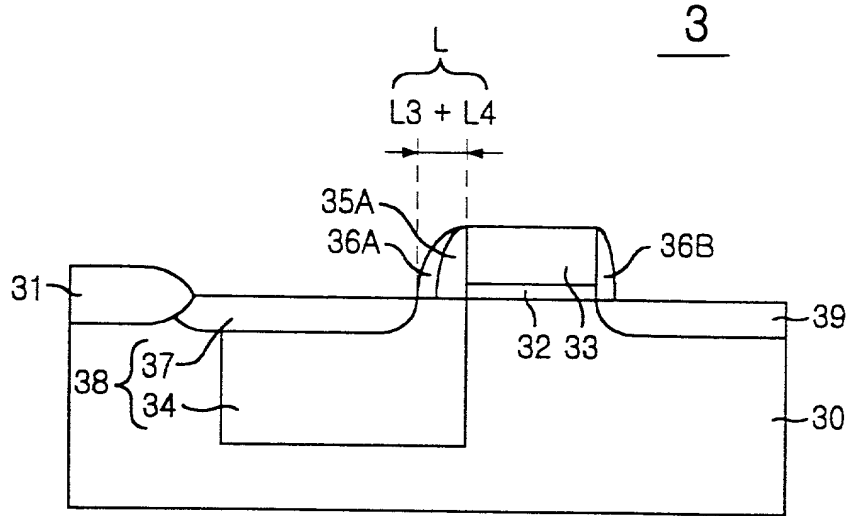


FIG. 4A

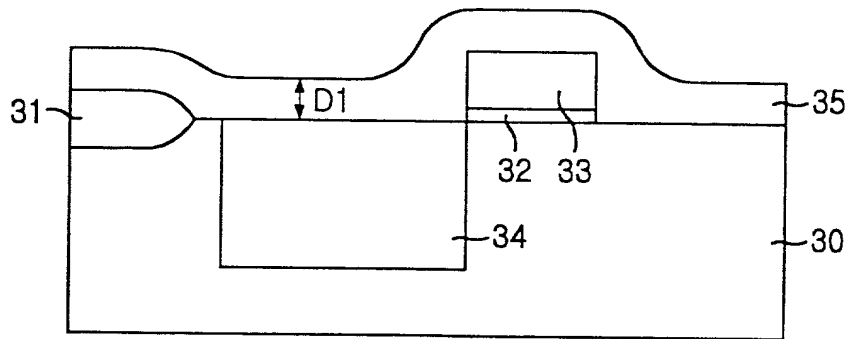


FIG. 4B

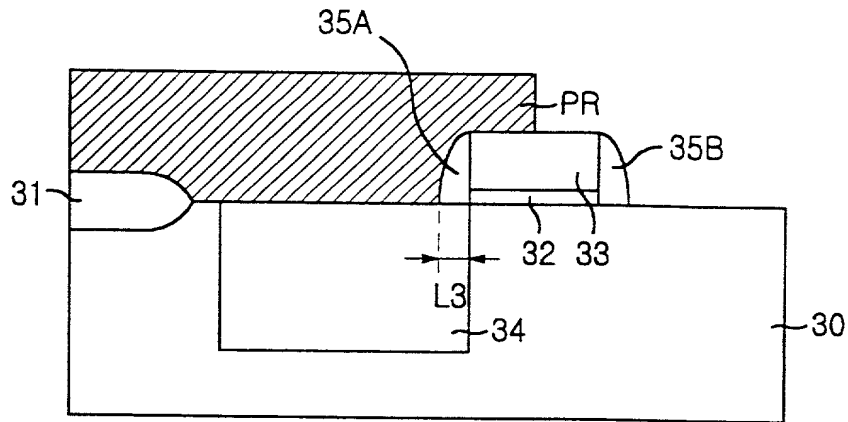


FIG. 4C

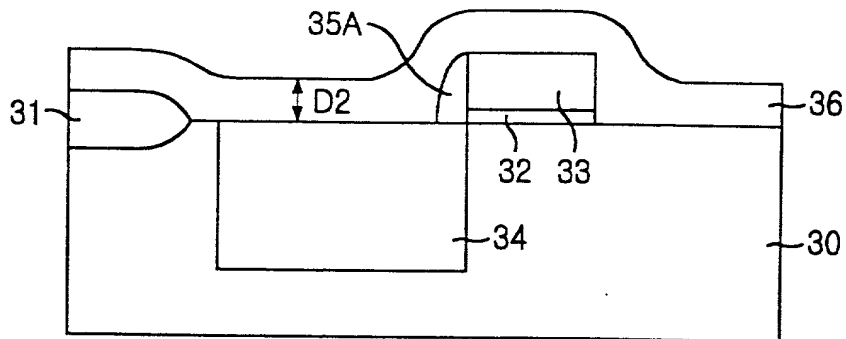


FIG. 4D

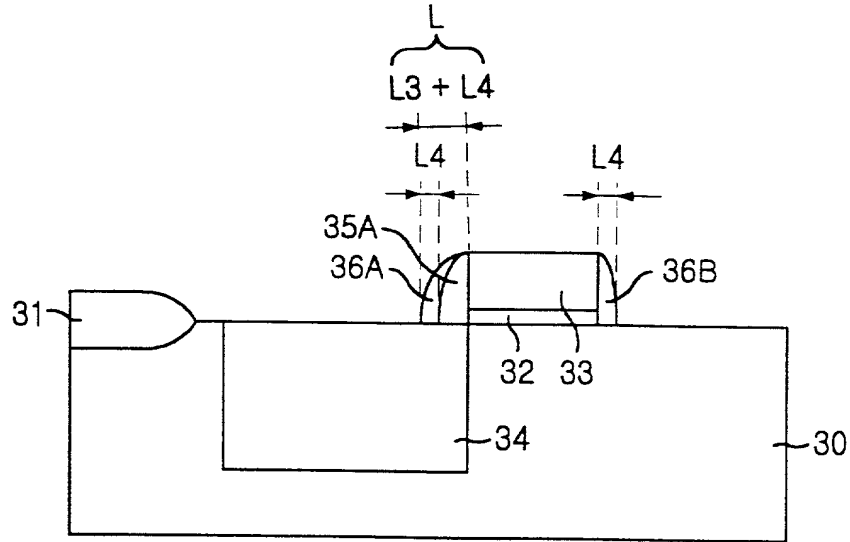


FIG. 4E

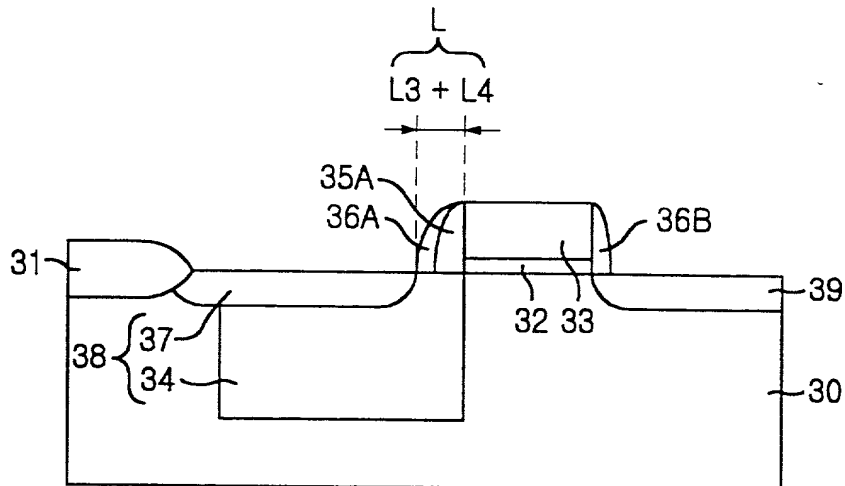


FIG. 5A

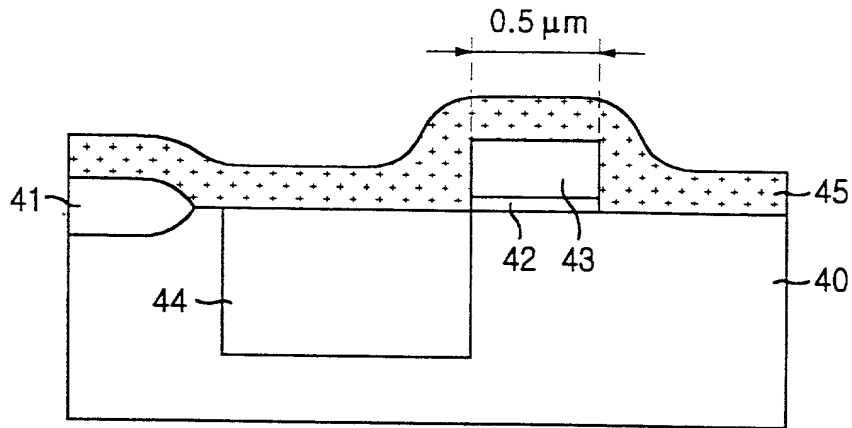


FIG. 5B

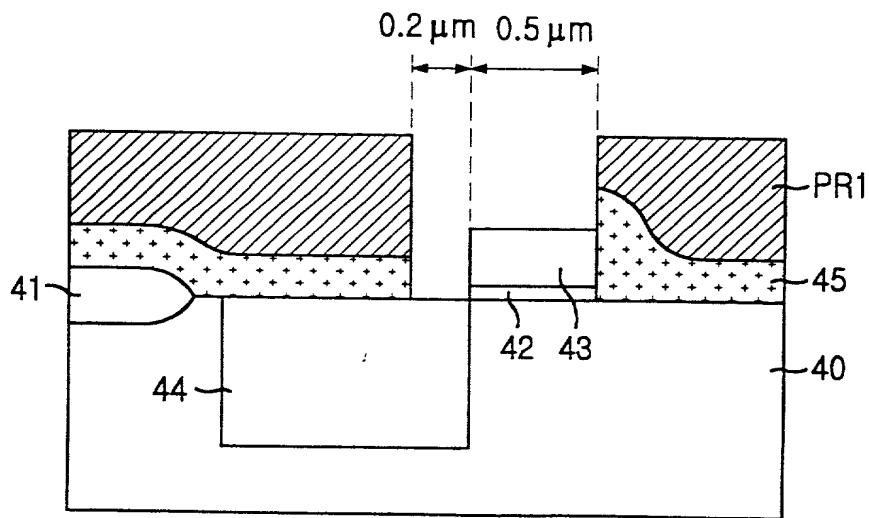


FIG. 5C

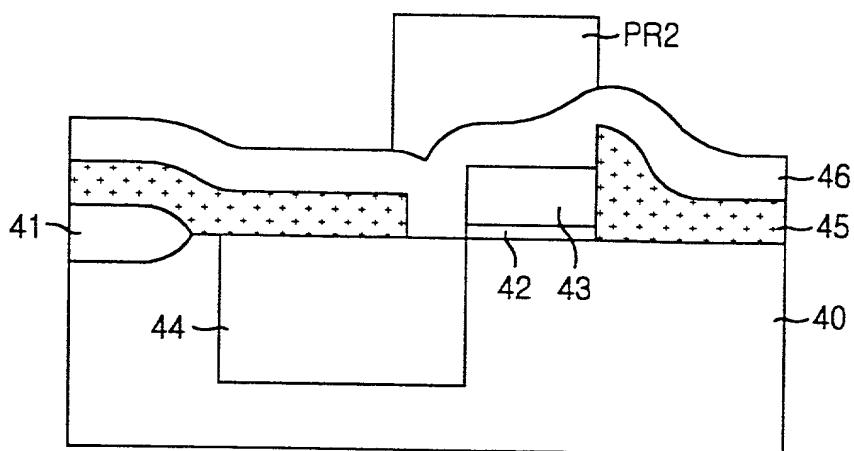


FIG. 5D

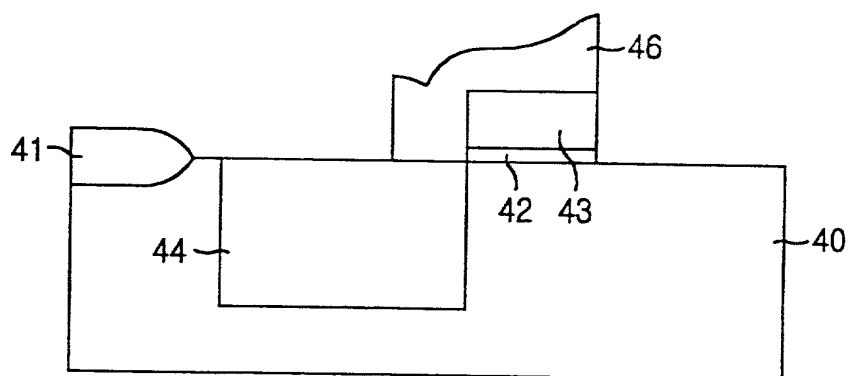


FIG. 5E

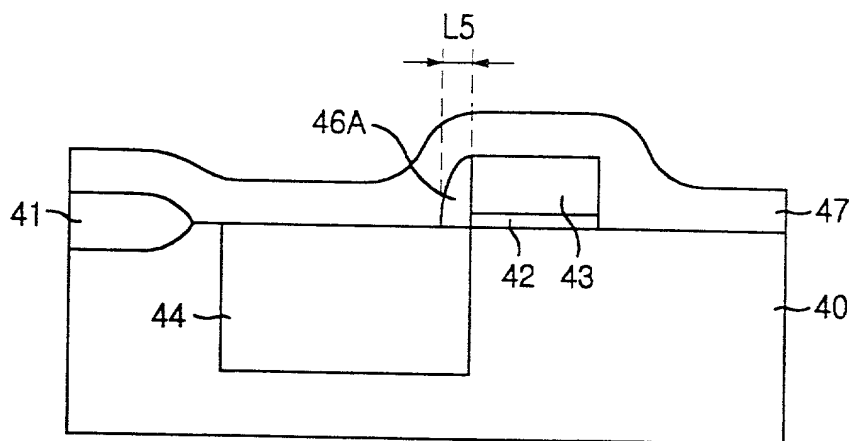
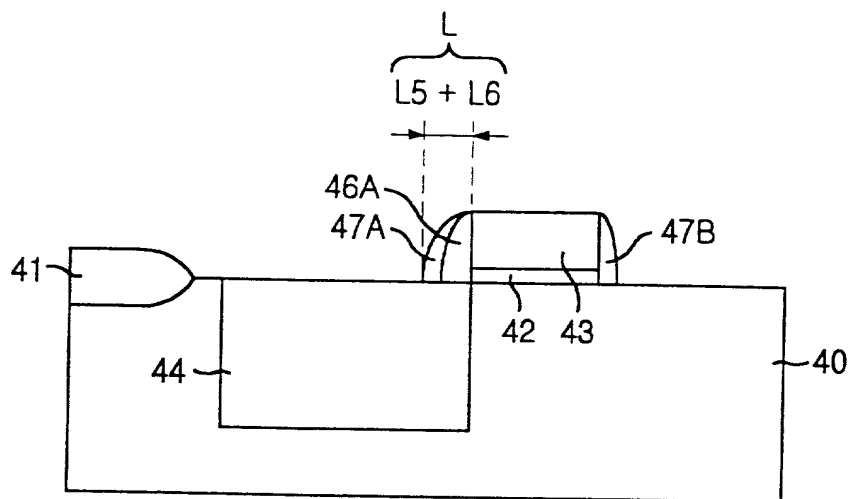


FIG. 5F



This diagram shows a cross-sectional view of a semiconductor device. A substrate 40 is shown with a first gate electrode 41 on its top surface. A second gate electrode 42 is formed on the top surface of the substrate 40, positioned to the right of the first gate electrode 41. The second gate electrode 42 is divided into two regions, 46A and 47B, by a gap 43. A second gate insulating layer 44 is formed on the top surface of the substrate 40, covering the second gate electrode 42. A second channel region 48 is formed in the substrate 40, located between the first gate electrode 41 and the second gate electrode 42. A second source region 49 is formed in the substrate 40, located to the left of the first gate electrode 41. A second drain region 50 is formed in the substrate 40, located to the right of the second gate electrode 42. The length of the second gate electrode 42 is indicated by a dimension line labeled L, which is divided into two segments, L5 and L6. The length of the second channel region 48 is indicated by a dimension line labeled L'.